Replacement Sheets

Drawings

Applicant : IOAN DANCEA

Application/Control No. : 09/874,027

Title : METHOD AND VLSI CIRCUITS ALLOWING TO CHANGE DYNAMICALLY THE LOGICAL BEHAVIOUR

EXAMINER : FRED FERRIS, Patent Examiner
Simulation and Emulation, Art Unit 2128

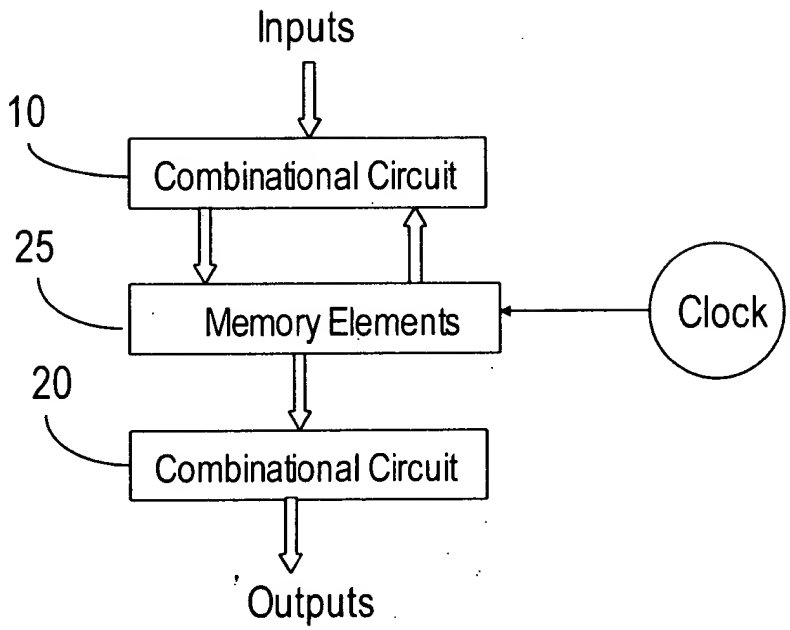


FIGURE 1
(Prior Art)

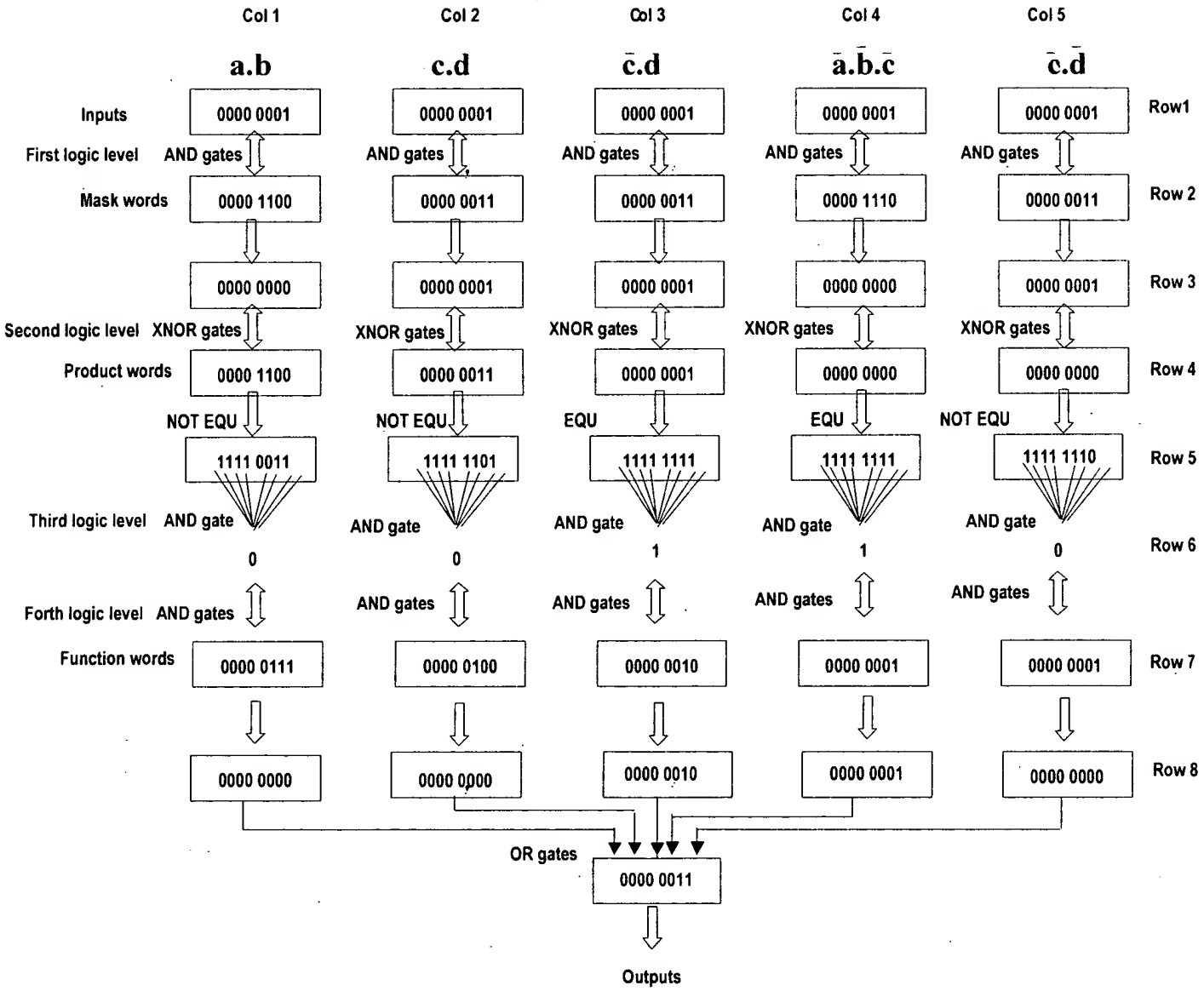

Col 1
Col 2
Col 3
Col 4
Col 5
a.b
c.d
c̄.d
ā.b̄.c̄
c̄.d̄
Inputs
0000 0001
First logic level AND gates
Mask words
0000 1100
0000 0011
0000 1110
Row1
Row 2
0000 0000
0000 0001
Row 3
Second logic level XNOR gates
Product words
0000 1100
0000 0011
Row 4
NOT EQU
EQU
1111 0011
1111 1101
1111 1111
1111 1110
Row 5
Third logic level AND gate
0
1
Row 6
Forth logic level AND gates
Function words
0000 0111
0000 0100
0000 0010
0000 0001
Row 7
Row 8
OR gates
Outputs

FIGURE 2A

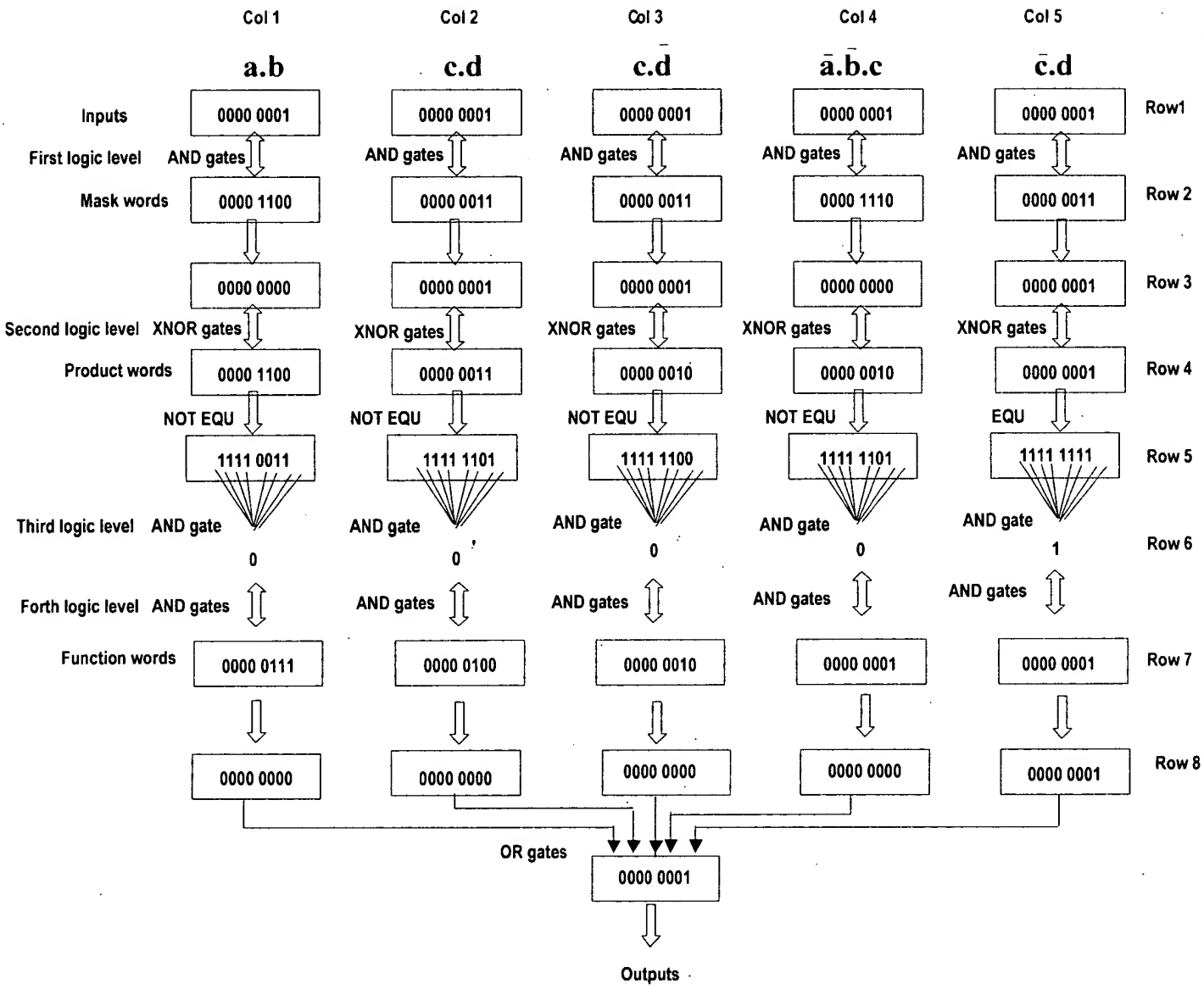

Col 1
Col 2
Col 3
Col 4
Col 5
a.b
c.d
c.d̄
ā.b̄.c
c̄.d
Inputs
First logic level
AND gates
Mask words
Second logic level
XNOR gates
Product words
NOT EQU
EQU
Third logic level
AND gate
Forth logic level
Function words
OR gates
Outputs
0000 0001
0000 1100
0000 0011
0000 1110
0000 0000
0000 0010
1111 0011
1111 1101
1111 1100
1111 1111
0
1
0000 0111
0000 0100
0000 0010
0000 0001
Row1
Row 2
Row 3
Row 4
Row 5
Row 6
Row 7
Row 8

FIGURE 2B

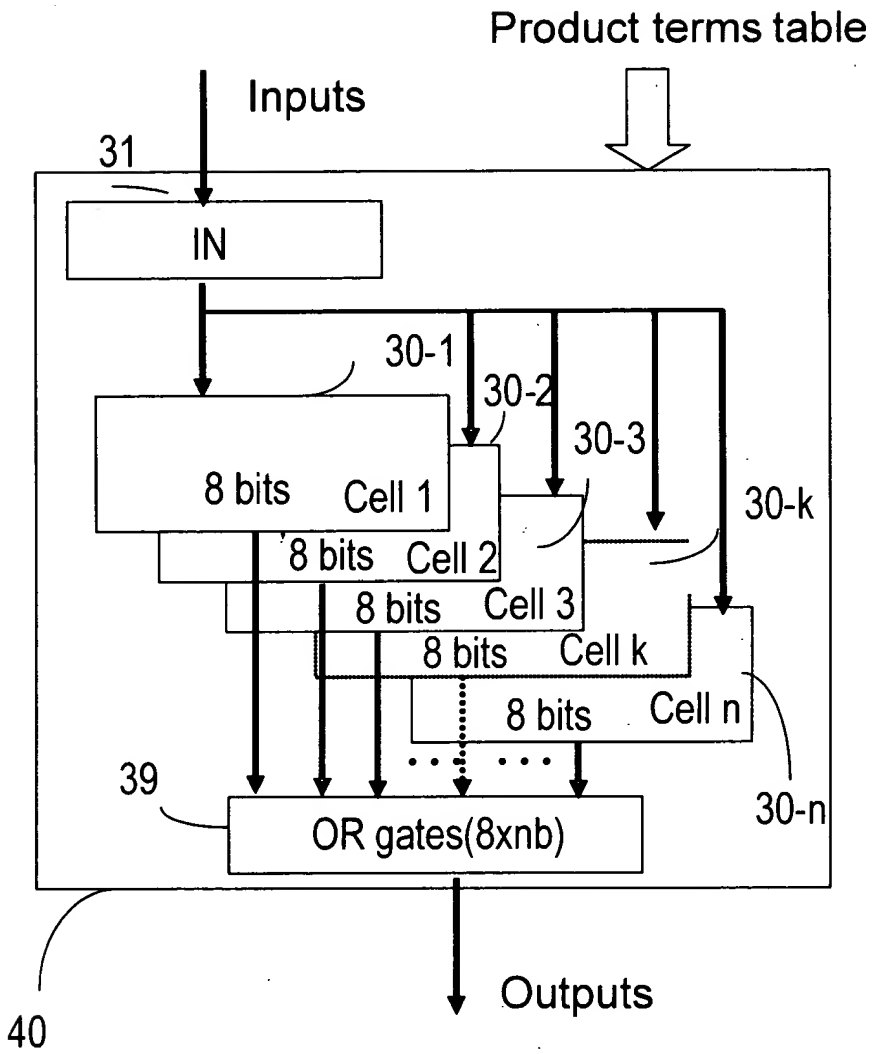

Product terms table
Inputs
31
IN
30-1
30-2
30-3
30-k
8 bits Cell 1
8 bits Cell 2
8 bits Cell 3
8 bits Cell k
8 bits Cell n
30-n
39
OR gates(8xnb)
Outputs
40

FIGURE 3

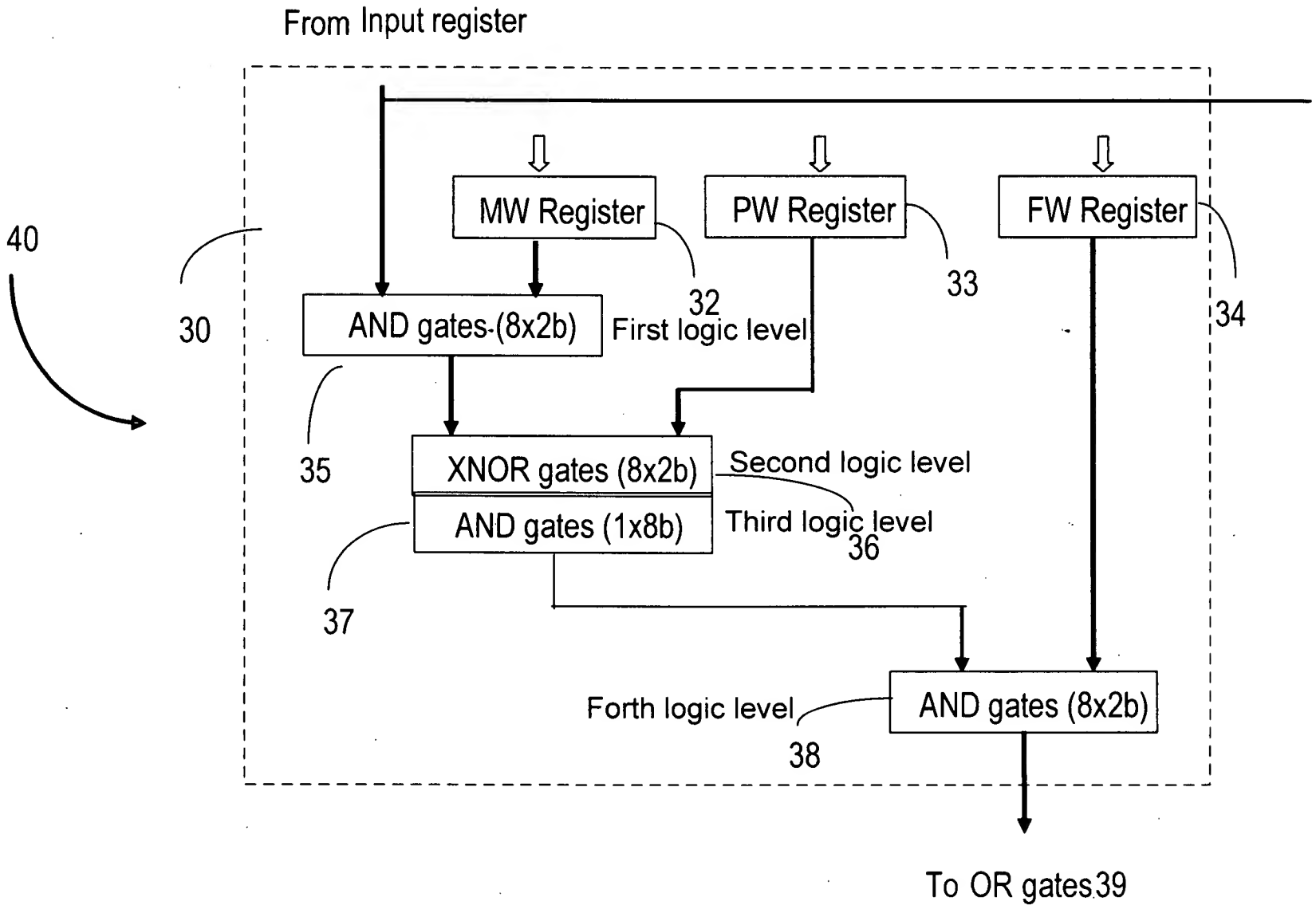

From Input register
40
30
MW Register
PW Register
FW Register
32
33
34
AND gates-(8x2b)
First logic level
35
XNOR gates (8x2b)
Second logic level
AND gates (1x8b)
Third logic level
36
37
Forth logic level
AND gates (8x2b)
38
To OR gates39

FIGURE 4

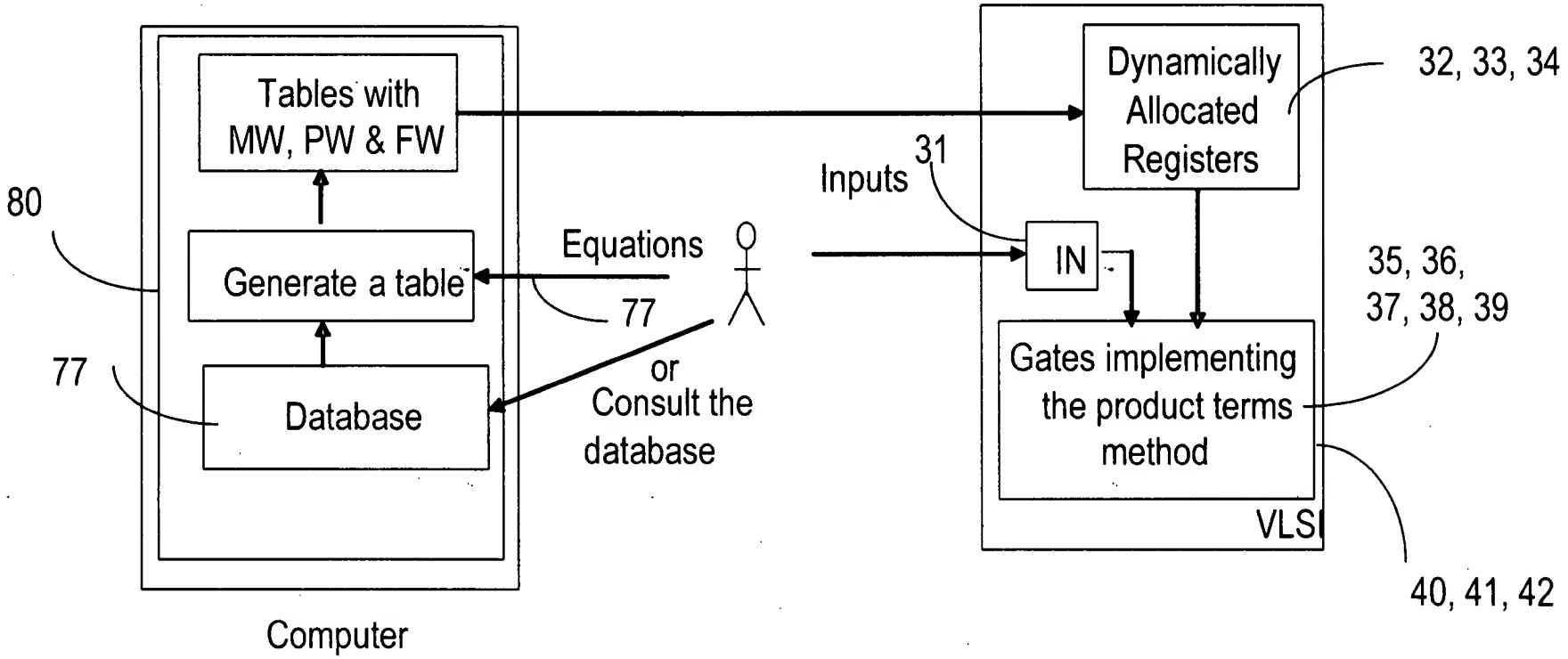

Tables with MW, PW & FW
80
Generate a table
77
Database
Computer
Equations
77
or Consult the database
Inputs
31
Dynamically Allocated Registers
32, 33, 34
IN
35, 36, 37, 38, 39
Gates implementing the product terms method
VLSI
40, 41, 42

FIGURE 5

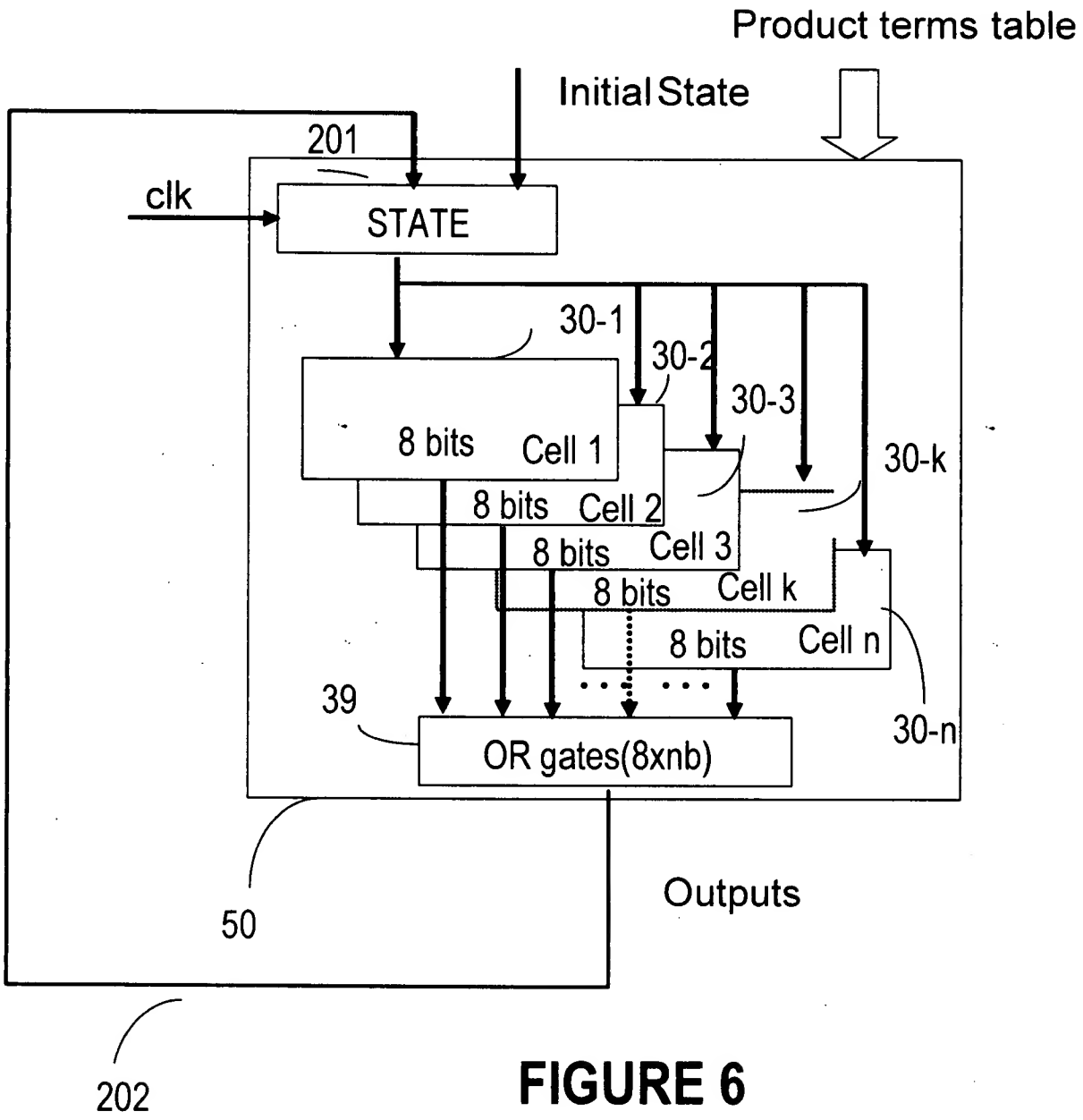

Product terms table
Initial State
201
clk
STATE
30-1
30-2
30-3
30-k
8 bits
Cell 1
8 bits
Cell 2
8 bits
Cell 3
8 bits
Cell k
8 bits
Cell n
39
OR gates(8xnb)
30-n
Outputs
50
202

FIGURE 6

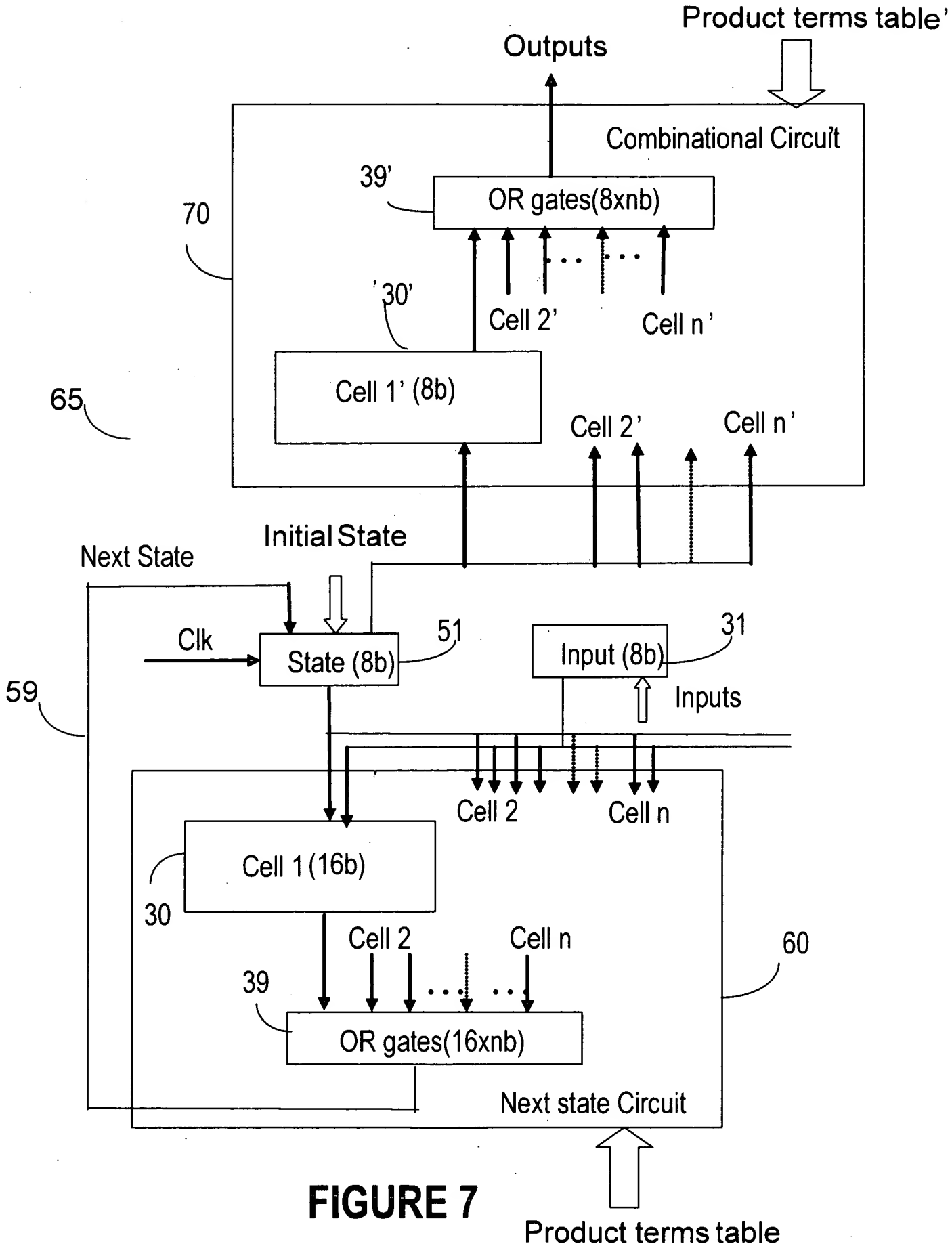

Product terms table'
Outputs
Combinational Circuit
39'
OR gates(8xnb)
70
'30'
Cell 2'
Cell n'
Cell 1' (8b)
65
Cell 2'
Cell n'
Initial State
Next State
Clk
State (8b)
51
Input (8b)
31
Inputs
59
Cell 2
Cell n
Cell 1 (16b)
30
Cell 2
Cell n
60
39
OR gates(16xnb)
Next state Circuit
Product terms table

FIGURE 7

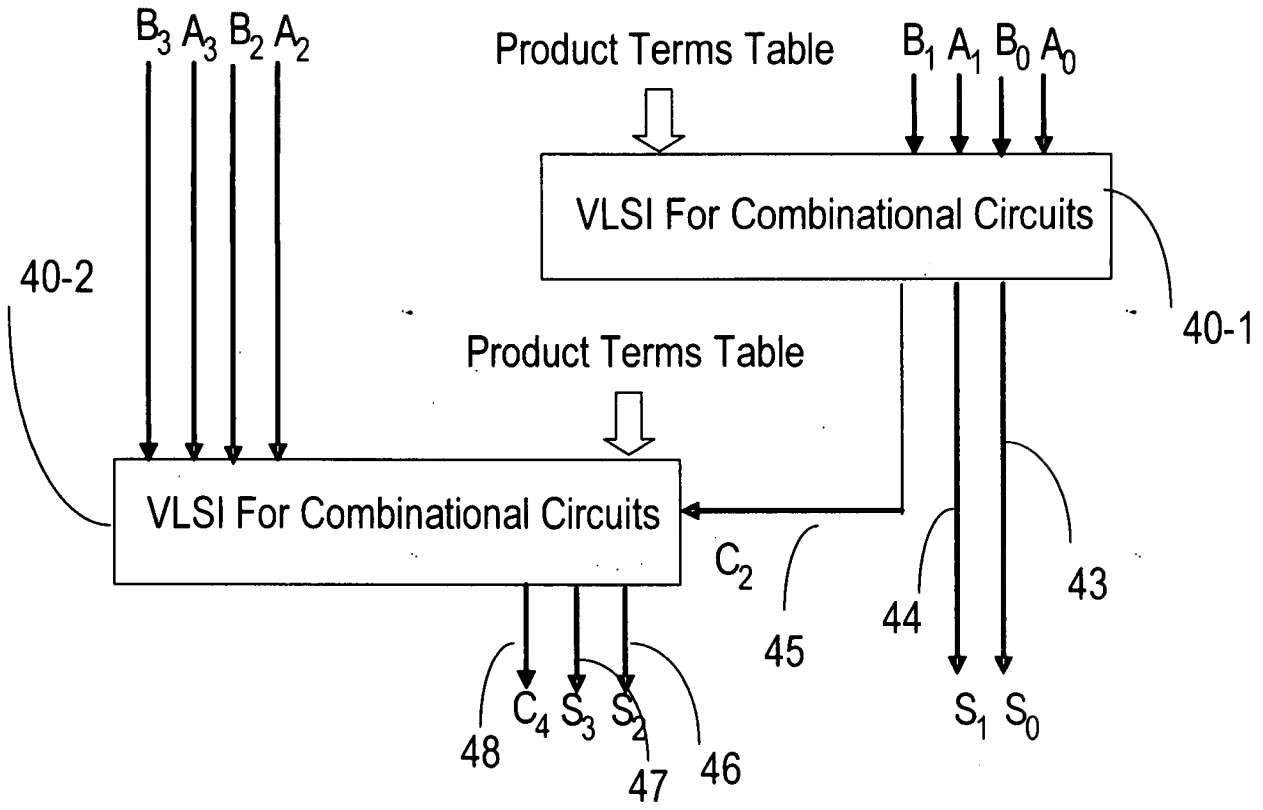

B3 A3 B2 A2
Product Terms Table
B1 A1 B0 A0
VLSI For Combinational Circuits
40-1
40-2
Product Terms Table
VLSI For Combinational Circuits
C2
45
44
43
C4 S3 S2
48
47
46
S1 S0

FIGURE 8

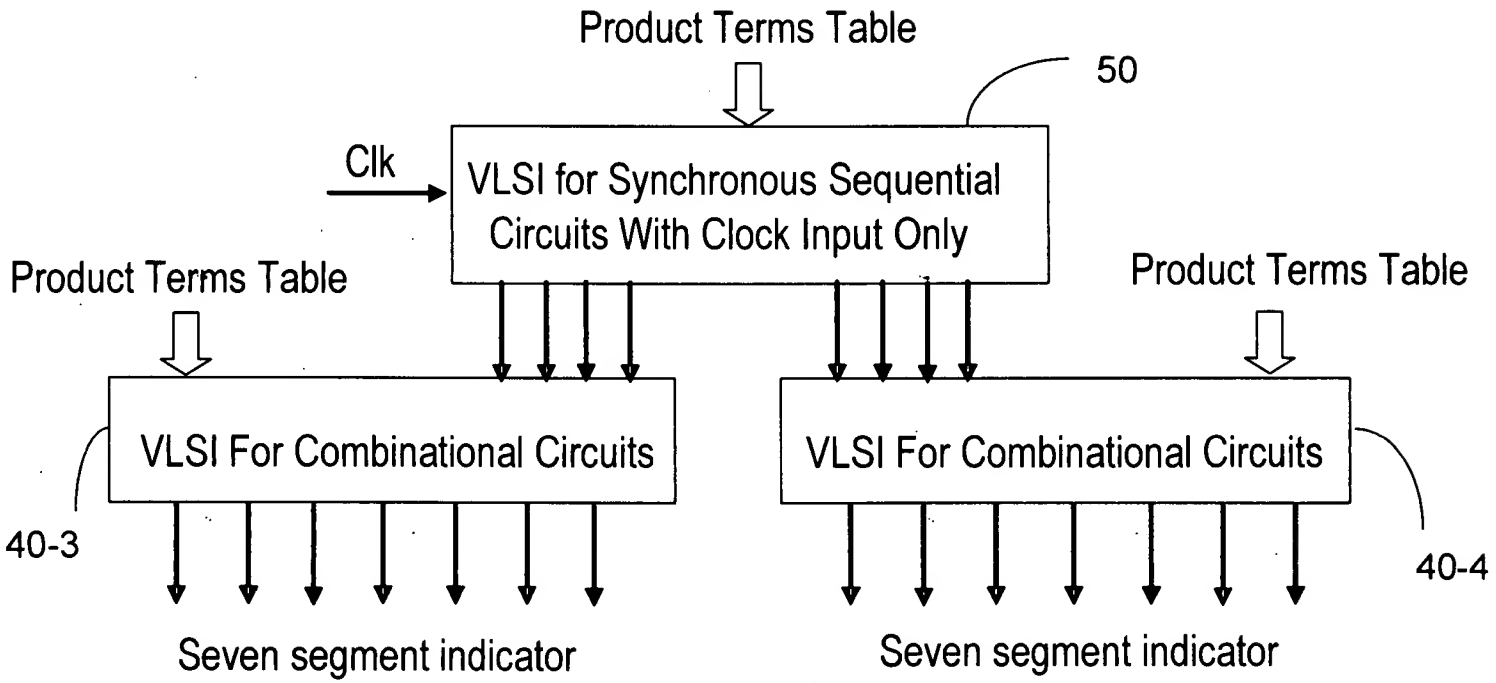

Product Terms Table
50
Clk
VLSI for Synchronous Sequential Circuits With Clock Input Only
Product Terms Table
Product Terms Table
VLSI For Combinational Circuits
VLSI For Combinational Circuits
40-3
40-4
Seven segment indicator
Seven segment indicator

FIGURE 9

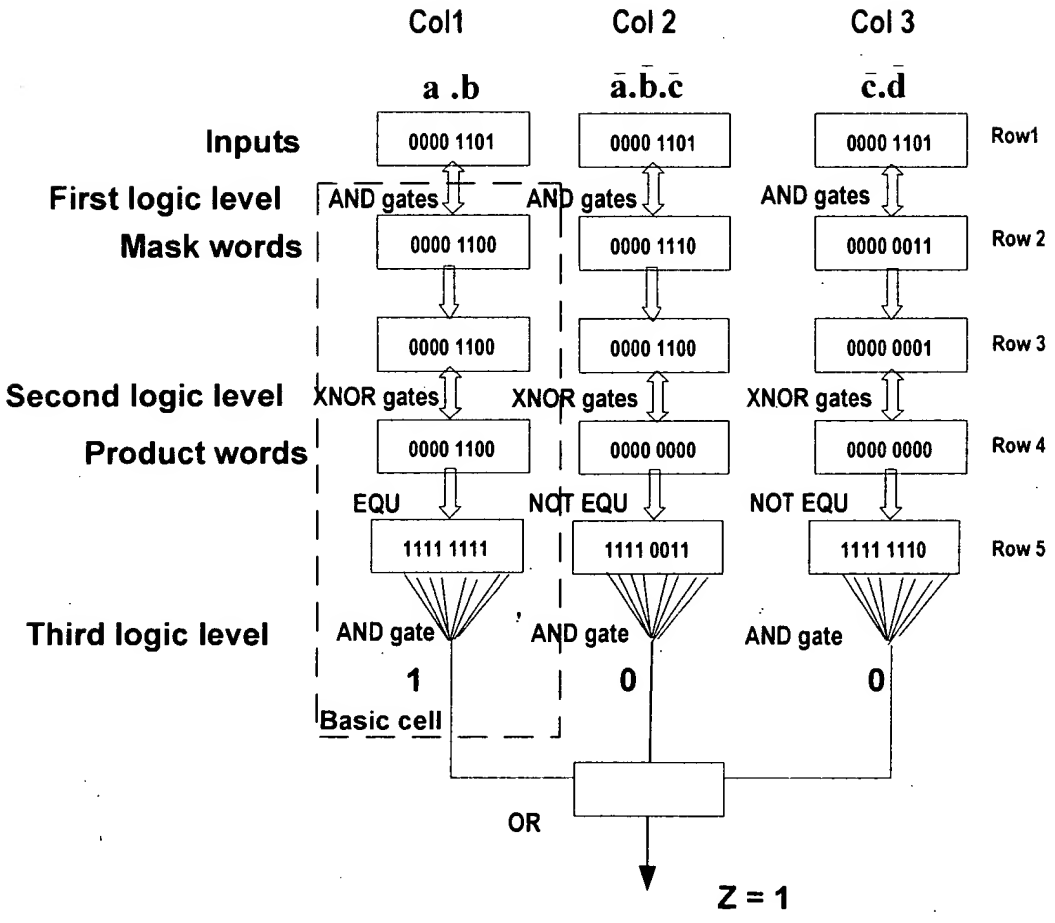

Col1
Col 2
Col 3
a .b
ā.b̄.c̄
c̄.d̄
Inputs
0000 1101
0000 1101
0000 1101
Row1
First logic level
AND gates
AND gates
AND gates
Mask words
0000 1100
0000 1110
0000 0011
Row 2
0000 1100
0000 1100
0000 0001
Row 3
Second logic level
XNOR gates
XNOR gates
XNOR gates
Product words
0000 1100
0000 0000
0000 0000
Row 4
EQU
NOT EQU
NOT EQU
1111 1111
1111 0011
1111 1110
Row 5
Third logic level
AND gate
AND gate
AND gate
1
0
0
Basic cell
OR
Z = 1

FIGURE 10

Replacement Sheet

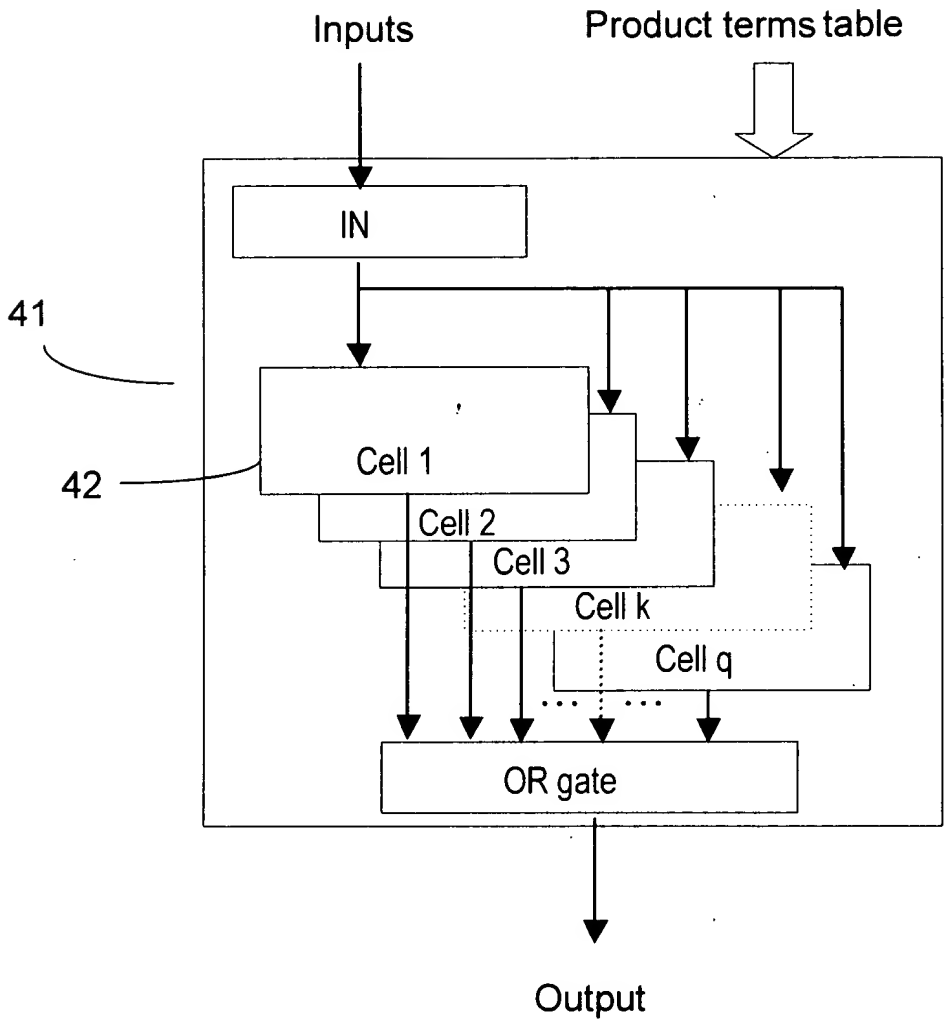


FIGURE 11

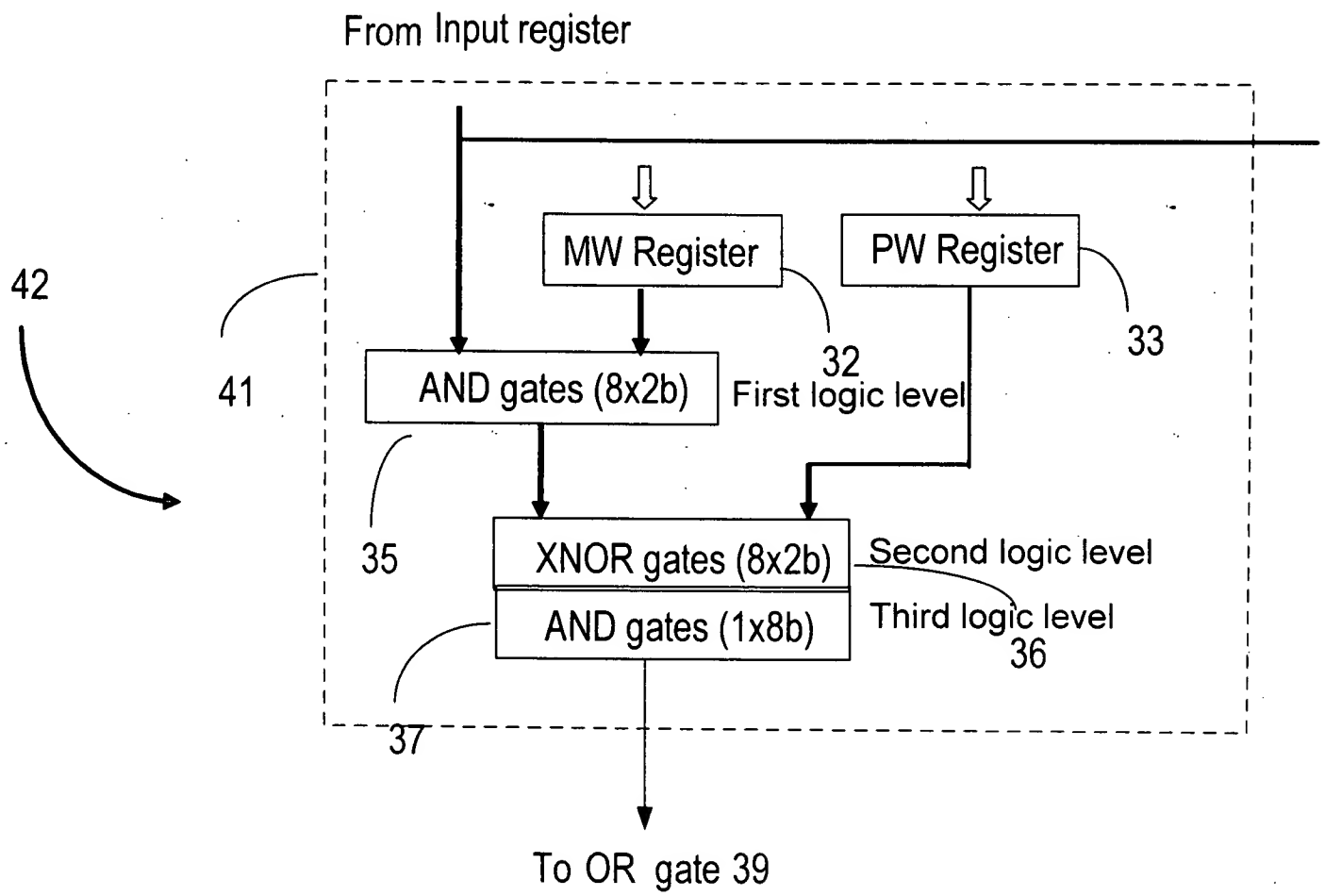
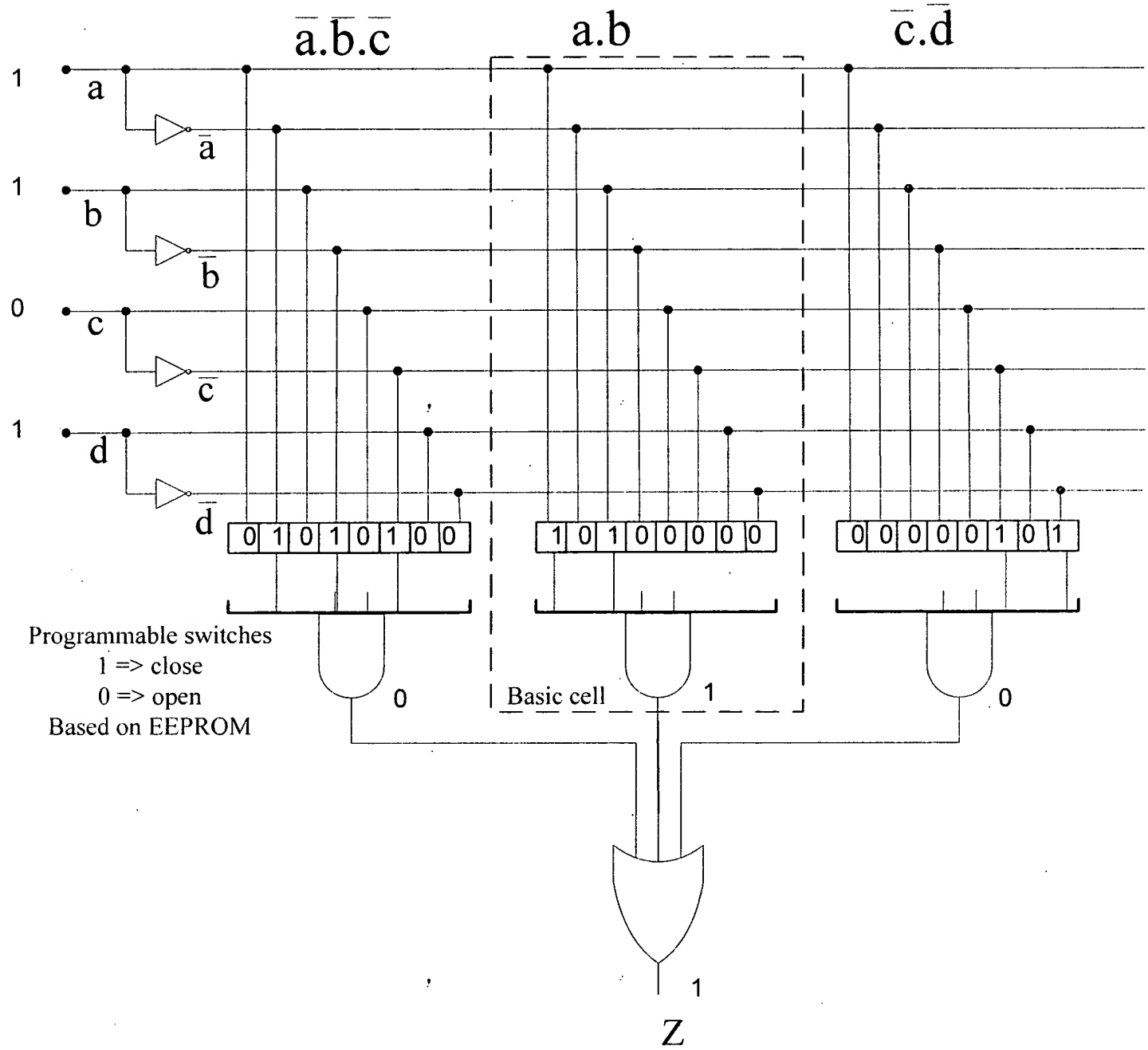

From Input register
42
41
MW Register
PW Register
32
33
AND gates (8x2b)
First logic level
35
XNOR gates (8x2b)
Second logic level
AND gates (1x8b)
Third logic level
36
37
To OR gate 39

FIGURE 12

Example showing a simplified cell in a first solution of CPLD device, based on PAL
(Like ALTERA MAX 7000)

PAL => one level of switches

$$Z = \bar{a}.\bar{b}.\bar{c} + a.b + \bar{c}.\bar{d}$$



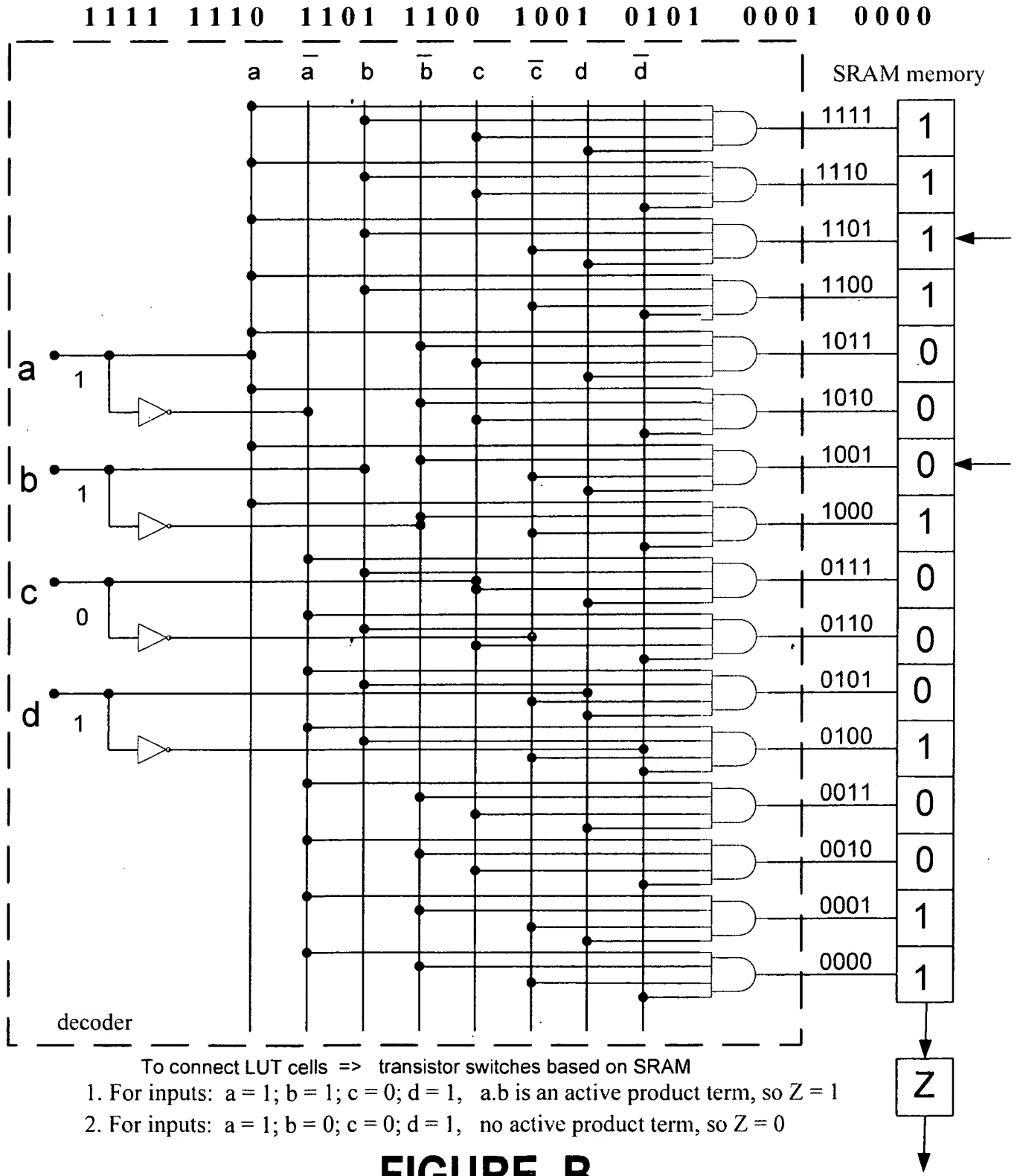
1. For inputs: a = 1; b = 1; c = 0; d = 1, a.b is an active product term, so Z = 1
2. For inputs: a = 1; b = 0; c = 0; d = 1, no active product term, so Z = 0

FIGURE A

Example showing a simplified cell in a first solution of FPGA device based on LUT
(Like ALTERA FLEX 10K)

$$Z = \bar{a}.\bar{b}.\bar{c} + a.b + \bar{c}.\bar{d}$$

$$Z = a.b.c.d + a.b.c.\bar{d} + a.b.\bar{c}.d + a.b.\bar{c}.\bar{d} + a.\bar{b}.\bar{c}.\bar{d} + \bar{a}.b.\bar{c}.\bar{d} + \bar{a}.\bar{b}.c.\bar{d} + \bar{a}.\bar{b}.\bar{c}.d$$



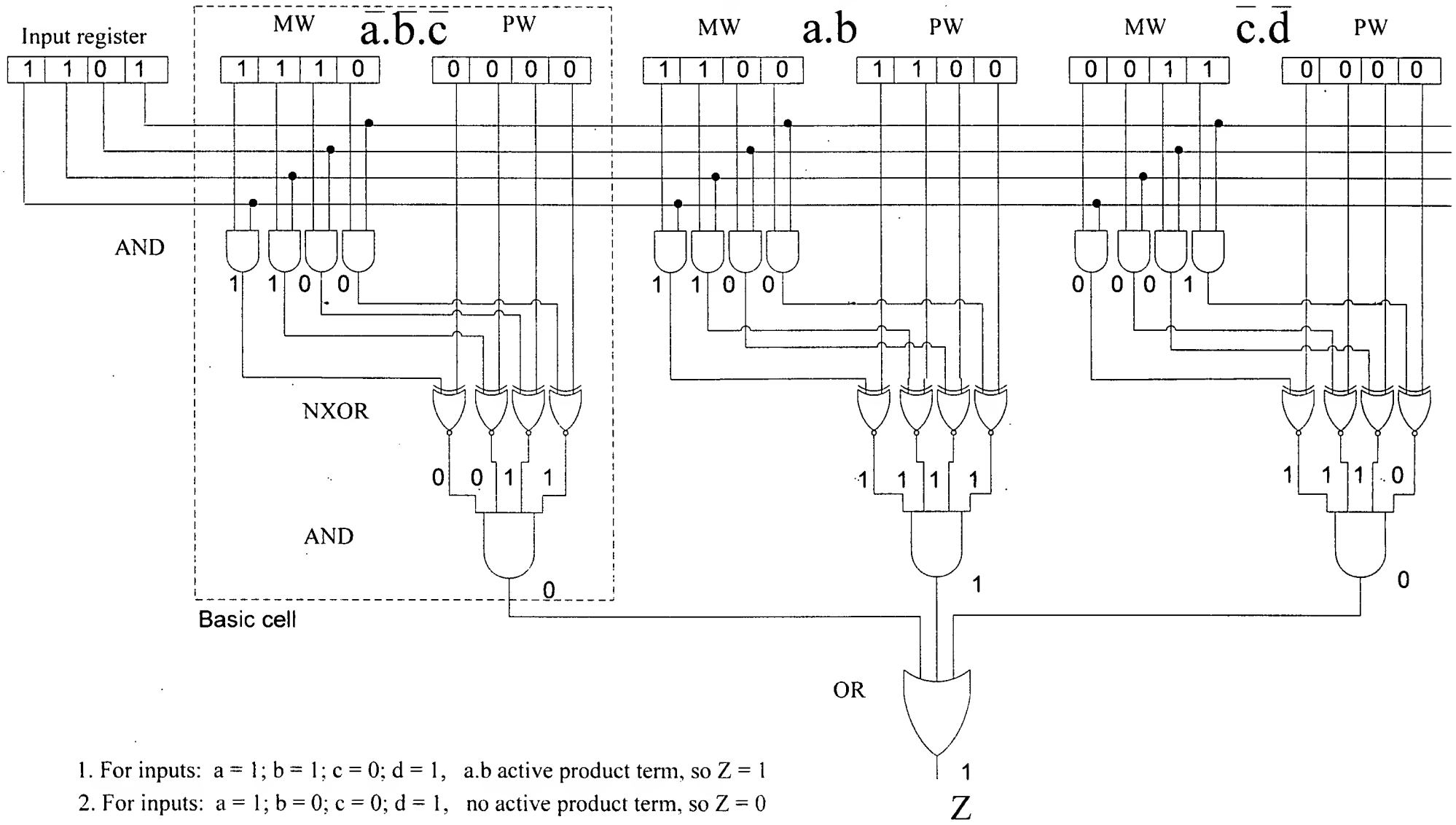
To connect LUT cells => transistor switches based on SRAM

1. For inputs: a = 1; b = 1; c = 0; d = 1, a.b is an active product term, so Z = 1
2. For inputs: a = 1; b = 0; c = 0; d = 1, no active product term, so Z = 0

FIGURE B

A simplified hardware structure for the first proposed solution, considering the same logical equation

$$Z = \bar{a}.\bar{b}.\bar{c} + a.b + \bar{c}.\bar{d}$$



1. For inputs: a = 1; b = 1; c = 0; d = 1, a.b active product term, so Z = 1
2. For inputs: a = 1; b = 0; c = 0; d = 1, no active product term, so Z = 0

FIGURE C